MANAV RACHNA
Vidyanatarikshat

MANAV RACHNA UNIVERSITY

(FORMERLY MANAV RACHNA COLLEGE OF ENGINEERING)
NAAC ACCREDITED 'A' GRADE INSTITUTION)
Declared as State Private University under section 2f of the UGC act, 1956

DEPARTMENT OF ECE

"T3 Examination, Dec 2018-19"

Semester: 3rd
Subject: PDE & Circuit Design
Branch: CSE
Course Type: CORE
Time: 3 Hrs.
Max. Marks: 100

Date of Exam: 04/12/2018
Subject Code: ECH 207-T
Session: II
Course Nature: HARD
Program: B. TECH.
Signature: HOD/Associate HOD:

~~Note:~~

PART -A

Q1.

a. Draw the XNOR gate logic using minimum no. of NAND gates only. (3)

b. Reduce using mapping the following expression and implement the real minimal expression in universal logic. (7)

$f = \sum m (0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$

OR

Q2.

a. Define the Fundamental Theorems of Boolean Algebra with example. (6)

b. Do the following: (4)

i. Covert $(678)_8 = (\quad)_{16}$

ii. Perform BCD addition of (91+81)

PART -B

Q3.

a. Implement the following function using 4*1 MUX (5)

$f(abc) = ab+b'c$

OR

a. Explain the Priority encoder with Truth Table and Logic Diagram. (5)

b. Draw the neat and clean diagram of BCD adder. (5)

PART –C *(Attempt any two)*

Q4.

a. Compare the Asynchronous and synchronous Counter. (5)

b. Design a Synchronous BCD counter using J-K flip-flop. (15)

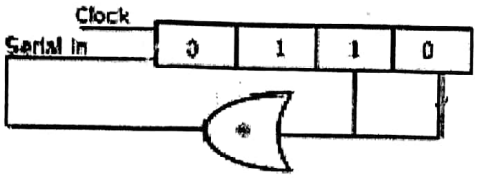
Q5.

a. Compare the sequential and combinational circuits. (5)

b. Explain the working of Universal register with diagram. (15)

Q6.

a. Examine the values of following right shift register after 5 clock pulses. (5)



b. What is the problem in JK flip-flop and how it can be removed, named it. (3)

c. Conversion of D flip-flop to JK flip-flop. (12)

PART –D (*Attempt any two)*

Q7.

a. Define the characteristics of logic family. (5)

b. What are the advantages of PLD devices over fixed function ICs and ASICs. (5)

c. Compare PROM, PLA, and PAL. (10)

Q8.

a. Implement the following Boolean function using PAL with 4 inputs and 3-wide AND-OR structure. Also write the PAL programming Table. (12)

$F1(A, B, C, D) = \sum m\ (2, 12, 13)$
$F2(A, B, C, D) = \sum m\ (7, 8, 9, 10, 11, 12, 13, 14, 15)$
$F3(A, B, C, D) = \sum m\ (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$
$F4(A, B, C, D) = \sum m\ (1, 2, 8, 12, 13)$

b. Compare the following: (8)

DRAM and SRAM
RAM and ROM

Q9.

a. Compare the ECL and TTL. (5)

b. Implement the following two Boolean functions with a PLA: (7)

$F1(A, B, C) = \sum m\ (0, 1, 2, 4)$
$F2(A, B, C) = \sum m\ (0, 5, 6, 7)$

c. Define the working of DTL with neat and clean circuit diagram. (8)

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