MANAV RACHNA vidyapeeth trust

MANAV RACHNA UNIVERSITY
FORMERLY MANAV RACHNA COLLEGE OF ENGINEERING
NAAC ACCREDITED 'A' GRADE INSTITUTION
Declared as State Private University under section 2f of the UGC act, 1956

DEPARTMENT OF ELECTRONICS & COMMUNICATION

"T2 Examination,October-2018"

Semester: 3rd
Subject: Principles of Digital Electronics & Ckt. Design
Branch: CSE
Course Type: Core
Time: 90 Minutes
Program: B.Tech

Date of Exam: 03/10/18
Subject Code: ECH207-T
Session: II
Course Nature: Hard
Max.Marks: 30
Signature: HOD/Associate HOD:

Note: Part A: All questions are compulsory. Each Question carries 2 marks. Part B: Attempt any two questions. Each Question carries 10 marks.

PART-A

Q1. (a) What is Multiplexer? How many 2:1 multiplexer are required to design a128:1 multiplexer?
(b) What is the difference between Encoder & Decoder?
(c) Give the Boolean expression and logic diagram for Half Subtractor.
(d) Design AND gate using multiplexer.
(e) Design Half Adder using only NAND gate.

PART-B

Q2. (a) Design Octal to Binary Encoder. [4]
(b) Simplify the following Boolean function by using tabulation method. [6]
$F(A,B,C,D)=\sum m(0,2,3,6,7,8,9,10,11,12,13)$

Q3. (a) Give the truth table for BCD to Excess-3 code converter. [2]
(b) Give the Boolean Expression for 4-bit binary to Gray Code converter. [5]
(C) Give the diagram for 4-bit parallel adder. [3]

Q4. (a) Design & Implement 2-bit Comparator using Logic gates. [6]
(b) Give the truth table for BCD to 7-segment Decoder. [2]
(C) Can Demultiplexer be used as a Decoder? Justify your answer. [2]

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