MANAV RACHNA
Vidyanand-e-Jivanam

MANAV RACHNA UNIVERSITY

(FORMERLY MANAV RACHNA COLLEGE OF ENGINEERING)
NAAC ACCREDITED 'A' GRADE INSTITUTION)
Declared as State Private University under section 2f of the UGC act, 1956

DEPARTMENT OF CST

"T3 Examination, May- 2019"

Semester: IV
Subject: COMPUTER ARCHITECTURE & ORGANISATION
Branch: CSE
Course Type: CORE
Time: 3 Hours
Max.Marks: 100

Date of Exam: 18/05/2019
Subject Code: CSH210-T
Session: II
Course Nature: HARD
Program: B.Tech
Signature: HOD/Associate HOD:

Note: Part A & B -Questions are compulsory. Each question carries 10 marks.
Part C & D- Attempt any two Questions. Each question carries 20 marks.

PART-A

Q. 1 (a) Perform the operation: [6]

$(11 \times 10)_2 + (C2)_{16} - (83.4)_9 + (95.34)_{10}$

And find out the result in Decimal Number system.

(b) Difference between Combinational & Sequential Circuits? [4]

PART-B

Q.2 (a) Write 14 bit control word for expression: R1←R2-R3? [2]

(b) Explain different types of Program Control instructions. [4]

(c) An instruction is stored at location 300 with its address field at location 301.The address field has the value 400.A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: [4]

i. Direct;
ii. Immediate;
iii. Relative;
iv. Register indirect.

PART-C

Q.3 (a) Design and explain the concept of expanded memory with the help of four RAMs (128 * 8 words) and a ROM (512 * 8 words). [5]

(b) i) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
ii) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? [5]

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(c) What are the different types of Interrupts? Explain how I/O interrupt can be handled with the help of interrupt cycle. [10]

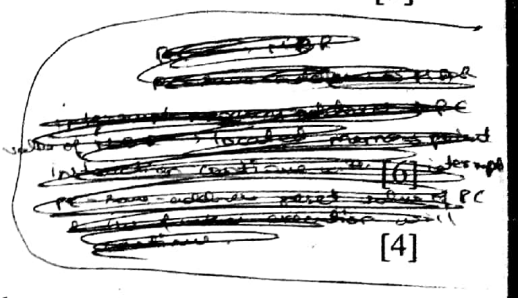
Q.4 (a) State the different Modes of Transfer. Explain working of DMA controller with the help of block diagram. [15]

(b) A cache memory needs an access time of 30ns and main memory 150 ns, what is average access time of CPU (assume hit ratio = 80%)? [5]

Q.5 (a) Design and explain RAM and ROM chip for 8085 microprocessor. [5]

(b) Expain the three different type of mapping procedures of cache memory with the help of diagram. [10]

(c) A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block, and word fields of the address format? [5]



PART-D

Q.6 (a) Explain working of Microprogrammed control organization. [6]

(b) Explain the Amdahl's Law of performance. [4]

(c) Formulate a six-segment Instruction Pipeline for a computer. Specify the operations to be performed in each segment. [10]

Q.7 (a) Explain Pipelining. Differentiate between Synchronous and Asynchronous pipelining. [8]

(b) Differentiate between Instruction format and Microinstruction format. [4]

(c) In certain scientific computations it is necessary to perform the arithmetic operation (Ai+Bi)(Ci+Di) with a stream of numbers. Specifiy a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 6. [8]

Q.8 (a) Explain the implementation of Control unit with Microprogram sequencer. [10]

(b) Explain various dependency problems in pipelining. [4]

(c) Differentiate between parallelism & pipelining. Also explain the goals of parallelism. [6]

Address Content