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wisdom unleashed

MANAV RACHNA UNIVERSITY
(FORMERLY MANAV RACHNA COLLEGE OF ENGINEERING)
NAAC ACCREDITED & GRADE INSTITUTION
Declared as State Private University under Section 2f of UGC Act, 1956

DEPARTMENT OF COMPUTER SCIENCE AND TECHNOLOGY

"T2 Examination, March2019"

Semester: 4th
Subject: COMPUTER ARCHITECTURE & ORGANISATION
Branch: CSE
Course Type:Core
Time: 1 Hour 30 Min.
Max Marks: 30

Date of Exam:12/03/19
Subject Code:CSH210 T
Session: II
Course Nature: Hard
Program: B.Tech
Signature: HOD/Associate HOD: for HOD

Note: Part A: Each Question carries 2 marks.
Part B: Attend any two Questions. Each Question carries 10 marks.

Part-A

Q1(a) Explain Control Word with help of block diagram.
(b) Differentiate between RISC & CISC computers.
(c) Explain Instruction set formats (fixed, variable, hybrid)
(d) What is the purpose of using Addressing Modes?
(e) Differentiate between Hardwired &Micro programmed control unit.

Part-B

Q2. (a) Discuss Detail data path of a typical register based CPU. Explain Fetch-Decode-Execute Cycle with diagrams. (10)

Q3. (a) Differentiate between Register stack & Memory stack organization. (5)
(b) Write a program to evaluate the following arithmetic statement using: (5)

((A+B) *(C+D))/E

(i) Three address instruction
(ii) Two address instruction
(iii) One address instruction
(iv) Zero address instruction
(v) RISC instruction

Q4. (a) Explain different types of Data transfer & Data manipulation instructions. (5)
(b) An instruction is stored at location 500 with its address field at location 501.The address field has the value 600.A processor register R1 contains the number 100. Evaluate the effective address if the addressing mode of the instruction is: (5)

i. Direct;
ii. Immediate;
iii. Relative;
iv. Register indirect;
v. Index with R1 as the index register;

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