MANAV RACHNA vidyanketan

MANAV RACHNA UNIVERSITY

DEPARTMENT OF COMPUTER SCIENCE & TECHNOLOGY

"T1 Examination, February-2019"

Semester: IV
Subject: COMPUTER ARCHITECTURE & ORGANISATION
Branch: CSE
Course Type: Core
Time: 90 Minutes
Program: B.Tech

Date of Exam: 04/02/19
Subject Code: CSH210-T
Session: II
Course Nature: Hard
Max.Marks:30
Signature: HOD/Associate HOD:

Note: Part A: All questions are compulsory. Each Question carries 2 marks.
Part B: Attempt any two questions. Each Question carries 10 marks.

PART-A

Q1. (a) Explain Binary representation of integers in Computer? (2)
(b) What are Performance Metrics? (2)
(c) State and prove De-Morgan's Law? (2)
(d) Difference between D Flip flop & T Flip flop? (2)
(e) Simplify the following Boolean postulate E= (a'+b').(a'+b).(a+b') (2)

PART-B

Q2. (a) Write a note on Store Program Control Concept? (5)

(b) Perform the operation: (5)
$(11 \times 10)_2 - (B2)_{16} + (25.74)_{10}$
And find out the result in Decimal Number system.

Q3. (a) Explain Decoders? Construct a 4 x 16 decoder, using two 3 x 8 decoders. (5)

(b) Explain Multi-level viewpoint of a machine with diagram. (5)

Q4. (a) Flynn's Classification divides computers in four major groups. Justify the statement. (5)

(b) Simplify the following Boolean expression: (5)

F= Σm (0, 3, 4, 5, 7) + Φ (8, 9, 10, 11, 12, 13, 14, 15) in canonical SOPs and implement them using basic gates.

IBM-360 IBM-310

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Von Neuman